

Synchronized window comparator eliminates error

SERGEY VELICHKO, CONSULTANT, BOSIE, ID

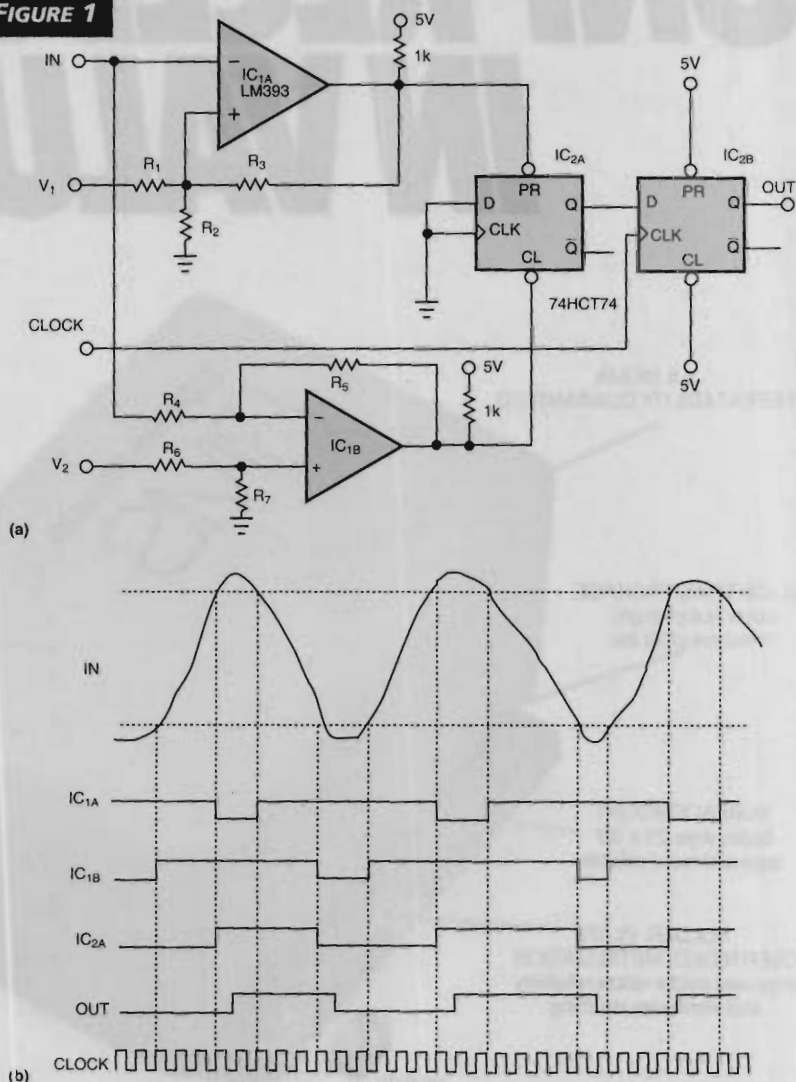
Precision A/D converters need a window comparator. The window comparator in Fig 1a is synchronized to the clock signal. This synchronization eliminates errors that could arise when the input signal crosses the high or low threshold (Fig 1b) unsynchronized to clock.

In operation, comparator IC_{1A} sets flip-flop IC_{2A} high when the input signal rises above the high threshold. Inverting comparator IC_{1B} sets flip-flop IC_{2B} low when the input signal descends past the low threshold. The second flip-flop, IC_{2B} , synchronizes the first flip-flop's output to the rising edge of the clock signal. Obviously, the clock signal must be significantly higher in frequency than the input signal to avoid problems with metastability.

The values for R_2/R_3 and R_4/R_5 determine the hysteresis for the comparators. Customary values for R_2 and R_3 are 10 k Ω and 1 M Ω for R_4 and R_5 . Reference-voltage V_1 , R_1 , and R_2 determine this high threshold. Similarly, reference-voltage V_2 , R_6 , and R_7 set the low threshold. (DI #1693)

To Vote For This Design, Circle No. 331

FIGURE 1



The output of this window comparator is synchronous with the clock signal.

Token passing fits large counters into CPLDs

CHRIS JONES AND DAVID JOHNSON, CYPRESS SEMICONDUCTOR CORP, SAN JOSE, CA

Fitting a large, loadable counter into a complex FLD (CPLD) while operating at the device's maximum frequency requires a few tricks. Fig 1 shows a 40-bit, loadable counter with a ter-

minal-count output. The problem with fitting this design into a CPLD is that the design exceeds the usual number of logic-block inputs, which is 36 or fewer. Normally, for the